PTO/SB/05 (12/97)

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Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**TI-24742**
First Named Inventor or Application Identifier	**Glen D. Wilk et al.**
Title	**Low Temperature Method For Forming A Thin, Uniform Oxide**
Express Mail Label No.	**EM 149073085 US**

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

1. [+] *Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [+] Specification *[Total Pages* **18** *]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [+] Drawing(s) *(35 USC d113)* *[Total Sheets* **4** *]*
4. Oath or Declaration *[Total Pages* **2** *]*
   - a. [+] Newly Executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR §1.63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [+] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3.73(b) Statement *(when there is an assignee)* [+] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [+] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [+] Preliminary Amendment
13. [+] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: / .

Prior application information: ***Examiner*** _____ ***Group / Art Unit:*** _____

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

NAME	**David Denker** **Texas Instruments Incorporated**				
ADDRESS	**P.O. Box 655474, MS 3999**				
CITY	**Dallas**	*STATE*	**Texas**	*ZIP CODE*	**75265**
COUNTRY	**USA**	*TELEPHONE*	**972-917-4388**	*FAX*	**972-917-4418**

Name (Print/Type)	**David Denker**	*Registration No. (Attorney/Agent)*	**40,987**
Signature		*Date*	21 Oct, 98

Burden Hour Statement: This form is estimated to take 0 2 hours to complete. Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO. Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT	($) 834.00

Complete If Known	
Application Number	TBD
Filing Date	TBD
First Named Inventor	Glen D. Wilk et al.
Examiner Name	TBD
Group / Art Unit	TBD
Attorney Docket No.	TI-24742

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account,

Deposit Account Number: 20-0668

Deposit Account Name: Texas Instruments Incorporated

☒ Charge any additional fee required or credit any overpayment

☐ Charge all indicated fees and any additional fee required or credit any overpayment

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$790
106	330	206	165	Design filing fee	$
107	540	207	270	Plant filing fee	$
108	790	208	395	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$
				SUBTOTAL (1)	($)790

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	22	-20**=	2	x	22	=	44
Independent Claims	2	-3** =	0	x	82	=	0
Multiple Dependent						=	

**or number previously paid, if greater; For Reissue, see below

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent Claims in excess of 3
104	270	204	135	Multiple dependent claims in excess of 3
109	82	209	41	**Reissue independent claims over original patent
110	22	210	11	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)44

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension of time within second month	
117	950	217	475	Extension of time within third month	
118	1,510	218	755	Extension of time within fourth month	
128	2,060	228	1,030	Extension of time within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a pubic use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt.	
581	40	581	40	Recording each patent assignment per properly (time number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1 129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) 0

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	David Denker	Reg. Number	40,987
Signature		Date: 2 October, 1998	Deposit Account User ID

Low Temperature Method for Forming a Thin, Uniform Oxide

This application claims the benefit of priority from the following U.S. applications:

Filing Date	Appl. #	Docket #	Title
7/31/97	TBD	TI-22960	Method For Thin Film Deposition On Single-Crystal Semiconductor Substrates

CROSS-REFERENCE TO RELATED APPLICATIONS

The following co-assigned U.S. patent applications are hereby incorporated by reference:

Docket	Serial No	Filing Date	Inventor	Title
TI-22960	TBD	7/31/97	Wilk *et al.*	Method For Thin Film Deposition On Single-Crystal Semiconductor Substrates

FIELD OF THE INVENTION

This invention pertains generally to forming thin oxides at low temperatures, and more particularly to forming thin oxides with high thickness uniformly.

BACKGROUND OF THE INVENTION

Semiconductors are widely used in integrated circuits for electronic devices such as computers and televisions. These integrated circuits typically combine many transistors on a single crystal silicon chip to perform complex functions and store data. Semiconductor and electronics manufacturers, as well as end users, desire integrated circuits that can accomplish more functions in less time in a smaller package while consuming less power. Miniaturization is a common approach to help meet these goals.

With increasing miniaturization, one concern is the thickness of the gate dielectric used in conventional CMOS circuits. The current drive in a CMOS transistor is directly proportional to the gate capacitance. Since capacitance scales inversely with gate dielectric thickness, higher current drive requires continual reductions in thickness for conventional dielectrics. Present technology uses silicon dioxide (SiO_2) based films with thicknesses near 5 nm. However, projections suggest the need for 2 nm (20 Å) films for future small geometry devices.

SUMMARY OF THE INVENTION

SiO_2 gate dielectrics in this thickness regime pose considerable challenges from a manufacturing perspective. Process control of the growth of a 2 nm film requires unprecedented thickness control. At these thicknesses direct tunneling through the SiO_2 may occur, although the effect of tunneling current on device performance may not preclude operation. Since the tunnel current depends exponentially on the dielectric thickness, small variations in process control may result in large variations in the tunnel current, possibly leading to reliability problems.

Another area of concern is the interface between the gate oxide and the channel region of the substrate. This silicon dioxide/silicon interface should be very flat and uniform to help limit interface scattering of electrons in the channel region.

Rapid thermal oxidation and furnace annealing are two current methods for forming gate oxides. However, current methods do not reliably produce gate oxides with the thickness uniformity and interface smoothness that will be needed to make devices with approximately 1.5 nm, 2 nm, or 2.5 nm gate oxides practical.

We disclose a low temperature method for forming a thin gate oxide on a silicon surface. This method comprises providing a partially completed integrated circuit on a semiconductor substrate with a clean silicon surface; and stabilizing the substrate at a first temperature. The method further includes exposing the silicon surface to an atmosphere containing ozone, while maintaining the substrate at the first temperature. In this method, the exposing step creates a first, uniformly thick, gate oxide film.

Preferably, exposing the silicon surface to an atmosphere containing ozone includes exposing the silicon surface to an atmosphere containing molecular oxygen, while irradiating at least a portion of the atmosphere with ultraviolet light, where the light transforms some of the oxygen to ozone. In some embodiments, the atmosphere further includes an inert gas, such as argon. Preferably, the ozone at the silicon surface is not in an excited energy state, such as a plasma. However, a plasma kept away from the wafer may be more acceptable.

In some embodiments, the clean silicon surface is atomically flat. Typically, the semiconductor substrate contains some areas that already have some structure, such as a field oxide. In some embodiments, the substrate has a plurality of clean, atomically flat, silicon surfaces. This might occur when the gate oxide is applied to surfaces exposed by etching "windows" in a layer overlying a silicon surface; or when overlying layers are added to the silicon surface, except where "islands" have been masked off.

In some embodiments, the first temperature is about 25 degrees C and the oxide film has a thickness of about 10 angstroms. In other embodiments, the first temperature may be up to about 200 degrees C, or even up to 600 degrees C. These temperatures will grow thicker oxides (up to about 35 angstroms) as shown in Fig. 3.

In another aspect of this method, the method further includes depositing a uniformly thick layer of silicon on the first oxide film to form a temporary silicon layer, the temporary silicon layer having a thickness no greater than the potential thickness of oxidizable silicon. This potential thickness is found by determining a planned substrate temperature for a second oxide film formation, the planned temperature no greater than about 200 degrees C. This planned temperature substantially determines the potential thickness of oxidizable silicon. After depositing the silicon, the method further includes exposing the temporary silicon layer to a second atmosphere containing ozone, while the substrate is at the planned substrate temperature. This exposing step oxidizes the temporary silicon layer to form a second, uniformly thick, oxide film extending to the first oxide film; thereby creating a single (combined), uniformly thick, oxide film.

In some embodiments, the method further includes stabilizing the substrate at the planned substrate temperature before the exposing step.

Brief Description Of The Drawings

Fig. 1 shows a low temperature method for forming a very thin, uniform oxide layer.

Fig. 2 shows a low temperature method for forming a very thin, uniform oxide layer.

Fig. 3 shows a relationship between time, oxide thickness, and temperature.

Fig. 4 shows a field-effect transistor using a thin, uniform oxide layer as the gate dielectric.

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Detailed Description

Fig. 1 outlines a method of using this invention to form a very thin, uniform SiO_2 gate dielectric on a silicon substrate. Initially, Si substrate **10** with a clean surface **12** is provided. Typically, this substrate **10** will include a partially completed integrated circuit with part of the surface **12** being either bare or hydrogen passivated silicon. This surface **12** may already have structures, such as field oxide regions, already formed upon it, and other structures, such as diffusion regions formed in the substrate beneath it.

We have found that a smooth, flat silicon surface tends to grow a more uniform oxide (particularly for very thin oxides) with this method. Thus, although a hydrogen terminated silicon surface usually produces acceptable results, many very thin, highly uniform silicon dioxide gate dielectrics prefer a silicon underlayer that approaches an atomically flat or atomically stepped surface. For our purposes, an atomically stepped surface will have a very low rms surface roughness, comparable to an atomically flat surface, in most areas. A wafer with an atomically stepped surface may have a series of adjacent flat surfaces (terraces). These terraces typically do not extend across a substrate wafer, and are not required to extend across a single device on a wafer. With very thin gate dielectrics, we sometimes prefer that adjacent terraces be connected by well-defined single- or double-atomic-height steps.

After the surface **12** is clean, but before exposure to an oxygen source, the substrate **10** temperature is stabilized at the oxidation temperature. This oxidation temperature substantially depends upon the thickness of the ozone-base oxide desired as shown in Fig. 3. This figure shows that for 1.0 nm oxides, the temperature should be near 25 degrees C. For a 2.0 nm oxide, the temperature should be approximately 500 degrees C. Similarly, 530 degrees C forms an approximately 2.5 nm oxide, while 550 degrees C forms an approximately 3.5 nm, high quality oxide. Fig. 3 was generated for UV-generated ozone in substantially pure oxygen at a 400 Torr O_2 pressure. Other ozone generation methods, or different oxygen pressures and/or concentrations may require adjustment of the temperature to yield a desired, precise oxide thicknesses.

This ability to grow precise, repeatable, usefully thick oxides at low temperatures greatly simplifies the temperature control problems. The ability to stabilize the whole wafer at the oxidation temperature allows for excellent process control, thus giving a uniform, repeatable oxidation thickness. Useful thermal oxides can be grown on wafers sitting in easily controlled furnaces. We have also found that this method is capable of producing oxides with good electrical properties. This ozone-based method can routinely achieve breakdown voltages above 10 MV/cm, such as 12 to 13 MV/cm.

The clean, temperature stabilized wafer with surface **12** is exposed to ozone **14**. We have found that introducing molecular oxygen to the reaction chamber and exposing the oxygen to a mercury lamp (particular with 183 nm and 253 nm emission lines), generates sufficient quantities of ozone. Other ultraviolet sources or other non-energetic ozone sources can be substituted for the mercury lamp generated ozone. Energetic ozone sources can be used, but it is preferable to keep the any excited ozone species from contacting the wafer. We have found that methods that allow an ozone plasma to contact the wafer form oxides with poor electrical properties, such as a significantly lower breakdown voltage. The ozone plasma methods also tend to exhibit poor uniformity and have repeatability problems. In our non-plasma ozone-based method, the oxygen/ozone **14** pressure can be varied from below a microtorr to several atmospheres. We have found that pressures between several hundred torr and one atmosphere provide a simple method to provide good results. If desired, the oxygen/ozone **14** can be mixed with an inert gas, such as argon.

This ozone-based process forms a very uniform, substantially thick silicon dioxide layer **16** on the exposed silicon surface **12**. This oxide layer **16** is much thicker than a conventional thermal oxide formed from exposing silicon to O_2 at the same temperature and time. Of even more importance, this oxide **16** is very repeatable and very uniform, primarily due to its self-limiting nature. When applied to a substantially flat silicon surface, this method repeatably produces SiO_2 layers with thickness uniformities better than 3% (better than 0.1 nm uniformity of an 3.0 nm thick oxide) across a 4 inch test wafer. Better heating uniformity can allow thickness uniformities below 1%. In fact, this method's oxide thickness uniformity will likely be limited in practice only by the heating uniformity, as opposed to the oxidation method itself. A typical transistor or capacitor layout will include a gate (or capacitor) electrode **21** superadjacent to the oxide **16**.

Fig. 3 shows that this method has a very slight time dependent component. However, for most temperature/thickness combinations, the oxidation rate has already slowed dramatically after 30 to 60 minutes. Thus, this process is nearly self terminating with reasonable reaction times. As such, this method can be relatively insensitive to large variations in oxidation time.

As the chart shows, higher temperatures will produce thicker oxides with this method. We have found that, if the thermal budget allows, we can easily produce high quality, 3.5 nm thermal oxides at only 550° C. Sometimes an artisan may prefer to use lower temperatures, but grow substantially thicker layers than shown in Fig. 3. For this case, we add extra steps as shown in Fig. 2, but still obtain a highly uniform oxide.

This variation involves first forming a highly uniform silicon dioxide layer **16** on a silicon surface **12** as described above. Next, a uniform silicon layer **18** is deposited on the silicon dioxide layer **16**. The thickness and uniformity of the final oxide layer will depend upon the thickness of the silicon layer **18**. Thus, silicon layer **18** should be formed with a well-controlled method, such as chemical vapor deposition or molecular beam epitaxy. This new silicon surface is then exposed to another ozone/oxygen atmosphere **14**, forming a single SiO_2 layer **20**. In this step, the total thickness of oxide layer **20** is determined by the thickness of the silicon **18** and the underlying SiO_2 layer **16**. However, the ozone allows complete oxidation of much thicker silicon layers than a straight oxygen atmosphere. If necessary, this silicon deposition and oxidation can be repeated to form thicker layers.

Fig. 4 shows a metal-oxide-silicon field-effect transistor (MOSFET) embodiment of this invention. Field-effect transistor **22** has four principal parts: a substrate **24**, a source **26**, a drain **28**, and a gate, where the gate includes the gate electrode **30** and thin silicon dioxide gate dielectric **32**. For an NMOS transistor **22**, p-type silicon substrate **24** includes n+ source **26** and n+ drain **28** regions. Gate dielectric **32** is a very thin, very uniform, silicon dioxide film, formed by using ozone to oxidize the cleaned silicon substrate **24**. MOSFET transistor **22** also includes sidewall spacers **34**, lightly doped drain (LDD) region **36**, and isolation region **38**. Those skilled in the art will recognize that these and other features may be used or left out, depending upon the particular function of the device and the intended processing flow.

These examples have shown NMOS transistors. Since the ozone-based thin gate oxide method is substantially insensitive to the doping profile of Si, no special modifications are required to implement this invention in PMOS devices or CMOS devices; or into SiO_2 based capacitors, which require a thin, very uniform dielectric with low electrical leakage and a high breakdown voltage.

Although this method provides substantial benefits when used to form thin oxide layers, it can also offer an improvement over typical methods for forming thicker high-quality oxide layers, such as a dielectric around the floating gate in a flash memory cell. If the thermal budget permits, this ozone-based method can be used to form relatively thick SiO_2 layers in a single pass, or even thicker layers in a layered approach like that described above. Although these thicker layers may require temperature of 600 or 700 degrees C, this variation of the ozone-based method allows lower temperature processing than conventional oxidation processes. Not only do these lower temperatures help the thermal budget, but the self-limiting nature of a ozone-based process improves process repeatability and oxide thickness uniformity, without sacrificing the oxide's electrical quality.

The present invention has been described with several sample embodiments. However, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.

We claim:

1. A low temperature method for forming a thin gate oxide on a silicon surface, the method comprising:

providing a partially completed integrated circuit on a semiconductor substrate with a clean, atomically flat, silicon surface;

stabilizing the substrate at a first temperature no greater than about 200 degrees C;

exposing the silicon surface to an atmosphere including ozone, while maintaining the substrate at the first temperature, wherein the exposing step creates a first, uniformly thick, gate oxide film.

2. The method of Claim 1, wherein exposing the silicon surface to an atmosphere including ozone comprises:

exposing the silicon surface to an atmosphere including molecular oxygen, while irradiating at least a portion of the atmosphere with an ultraviolet light, the light operative to transform some of the oxygen to ozone.

3. The method of Claim 1, wherein the atmosphere further comprises molecular oxygen.

4. The method of Claim 1, wherein the atmosphere further comprises an inert gas.

5. The method of Claim 1, wherein exposing the silicon surface to an atmosphere including ozone includes exposing the silicon surface to an atmosphere with less energy than a plasma.

6. The method of Claim **5**, wherein at least part of the atmosphere that does not contact the silicon surface includes an ozone plasma.

7. The method of Claim 1, wherein the atomically flat, silicon surface is an atomically stepped surface.

8. The method of Claim 1, wherein the semiconductor substrate includes a plurality of clean, atomically flat, silicon surfaces.

9. The method of Claim 1, further comprising forming a gate electrode on the gate oxide film

10. The method of Claim 1, wherein the first temperature is about 25 degrees C and the oxide film has a thickness of about 10 angstroms.

11. The method of Claim 1, wherein the first temperature is between 0 and 200 degrees C and the oxide film has a thickness between 5 and 20 angstroms.

12. The method of Claim 1, wherein the first temperature is about 200 degrees C.

13. The method of Claim 1, wherein the first temperature is about 200 degrees C and the oxide film has a thickness of about 12 angstroms.

14. The method of Claim 1, further comprising:

determining a planned substrate temperature for a second oxide film formation, the planned temperature no greater than about 200 degrees C; thereby substantially determining a potential thickness of oxidizable silicon;

depositing a uniformly thick layer of silicon on the first oxide film to form a temporary silicon layer, the temporary silicon layer having a thickness no greater than the potential thickness of oxidizable silicon;

exposing the temporary silicon layer to a second atmosphere including ozone, while the substrate is at the planned substrate temperature,

wherein the exposing step oxidizes the temporary silicon layer to form a second, uniformly thick, oxide film extending to the first oxide film; thereby creating a combined, uniformly thick, oxide film.

15. The method of Claim 14, further comprising:

stabilizing the substrate at the planned substrate temperature before the exposing step.

16. The method of Claim 14, further comprising:

repeating the determining, depositing, and exposing at the planned temperature steps at least once; thereby increasing the thickness of the combined oxide film.

17. The method of Claim 14, wherein the first temperature and the planned temperatures are about 25 degrees C and the combined oxide film has a thickness of about 20 angstroms.

18. A low temperature method for forming a thin gate oxide on a silicon surface, the method comprising:

providing a partially completed integrated circuit on a semiconductor substrate with a clean silicon surface;

stabilizing the substrate at a first temperature no greater than about 200 degrees C;

exposing the silicon surface to an atmosphere including ozone, while maintaining the substrate at the first temperature, wherein the exposing step creates a first, uniformly thick, gate oxide film; and

forming a gate electrode on the oxide film.

19. The method of Claim 18, wherein the clean silicon surface is a hydrogen terminated silicon surface.

20. The method of Claim 18, further comprising:

determining a planned substrate temperature for a second oxide film formation, the planned temperature no greater than about 200 degrees C; thereby substantially determining a potential thickness of oxidizable silicon;

depositing a uniformly thick layer of silicon on the first oxide film to form a temporary silicon layer, the temporary silicon layer having a thickness no greater than the potential thickness of oxidizable silicon;

exposing the temporary silicon layer to a second atmosphere including ozone, while the substrate is at the planned substrate temperature,

wherein the exposing step oxidizes the temporary silicon layer to form a second, uniformly thick, oxide film extending to the first oxide film; thereby creating a combined, uniformly thick, oxide film.

21. The method of Claim 20, further comprising:

stabilizing the substrate at the planned substrate temperature before the exposing step.

22. The method of Claim 20, further comprising:

repeating the determining, depositing, and exposing at the planned temperature steps at least once; thereby increasing the thickness of the combined oxide film.

Best Available Copy

Low Temperature Method for Forming a Thin, Uniform Oxide

ABSTRACT

This invention pertains generally to forming thin oxides at low temperatures, and more particularly to forming uniformly thick, thin oxides. We disclose a low temperature method for forming a thin, uniform oxide **16** on a silicon surface **12**. This method includes providing a partially completed integrated circuit on a semiconductor substrate **10** with a clean, hydrogen terminated or atomically flat, silicon surface **12**; and stabilizing the substrate at a first temperature. The method further includes exposing the silicon surface to an atmosphere **14** including ozone, while maintaining the substrate **10** at the first temperature. In this method, the exposing step creates a uniformly thick, oxide film **16**. This method is suitable for room temperature processing.

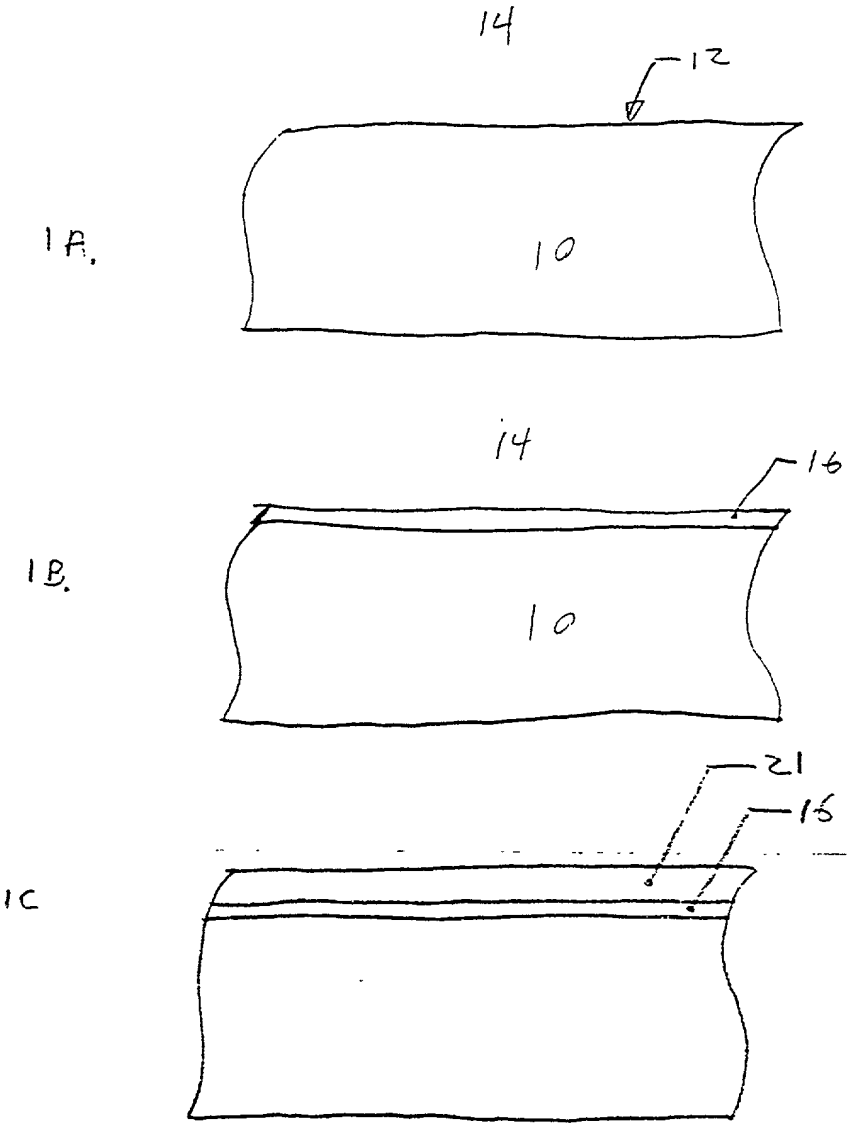
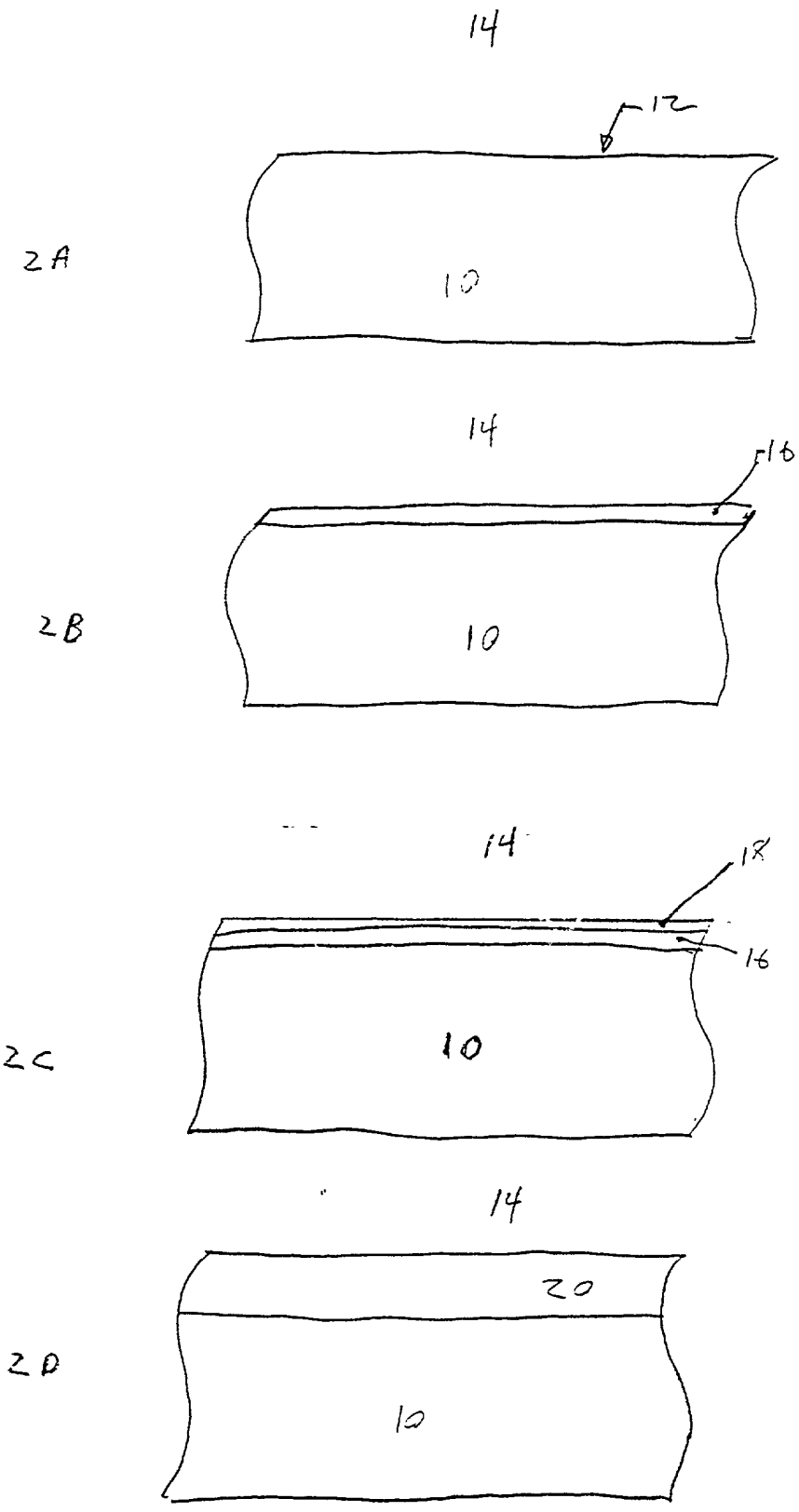


Figure 1

TI-24742



2A

2B

2C

2D

Figure 2

TI-24742

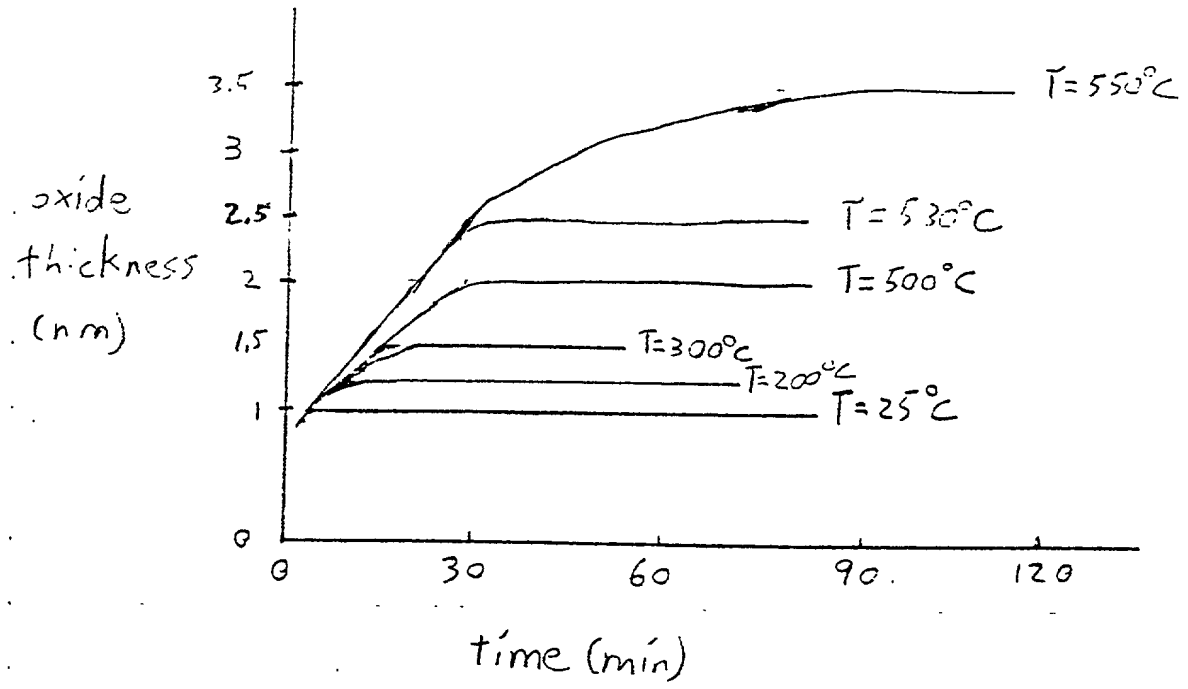


Fig. 3

TI-24742

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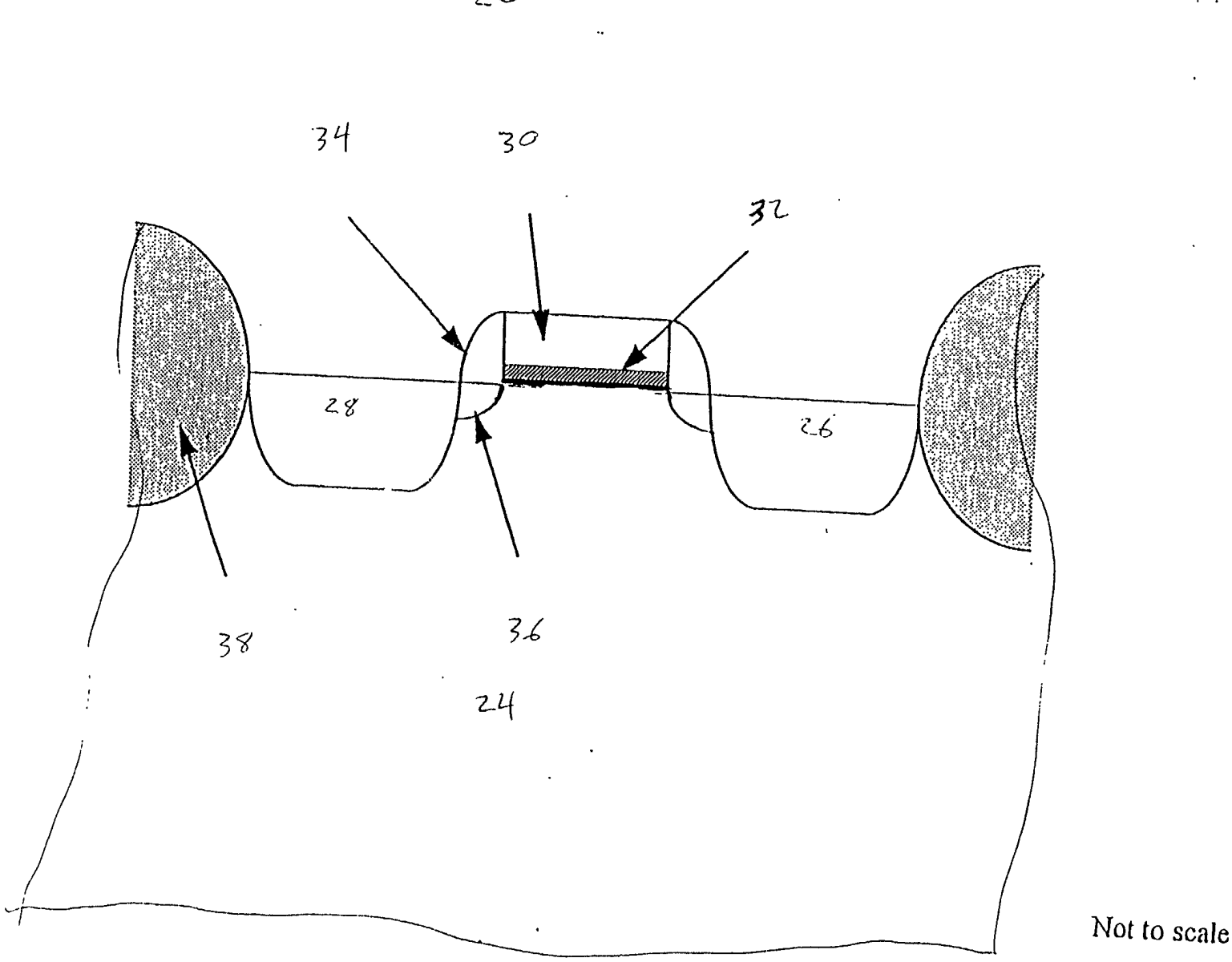
Fig. 4

TI-2474.2



Not to scale

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Wilk *et al.*	Docket:	TI-24742
Provisional Serial No.:	60/063,010	Examiner:	TBD
Serial No.:	TBD	Art Unit:	TBD
Provisional Filed:	10/23/97		
Filed:	Herewith		
For:	Low Temperature Method for Forming a Thin, Uniform Oxide		

PRELIMINARY AMENDMENT

MAILING CERTIFICATE UNDER 37 CFR § 1.8
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on

October 21, 1998.

Sue Short

Sue Short

September 28, 1998

Ass't Commissioner for Patents
Washington, DC 20231

Examiner:

Prior to examination and calculation of fees, please amend the above-identified application as follows:

IN THE SPECIFICATION:

On Page 1, lines 5-9, delete the table in its entirety and replace with the following:

Filing Date	Appl. No.	Title
7/31/97	08/904,009	Method For Thin Film Deposition On Single-Crystal Semiconductor Substrates
10/23/97	60/063,010	Low Temperature Method for Forming a Thin, Uniform Oxide

On Page 1, lines 14-19, delete the table in its entirety and replace with the following:

Filing Date	Appl. No.	Title
7/31/97	08/904,009	Method For Thin Film Deposition On Single-Crystal Semiconductor Substrates

On Page 9, line 7, after “sources” insert -- —including commercial ozone generators— --;

On Page 9, line 7, before “Energetic” insert --One example of a suitable commercial ozone generator is a barrier discharge ozonizer. --.

REMARKS

If Examiner has any further comments or suggestions, Applicants respectfully request that Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Respectfully submitted,

David Denker
Reg. No. 40,987

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-4388
Fax (972) 917-4418

ATTORNEY'S DOCKET NO.
TI-24742

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, and I believe that I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, and the preliminary amendment dated September 28, 1998.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations §1.56(a).

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States applications listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of these applications:

No. 08/904,009 filed 07/31/97 and No. 60/063,010 filed 10/23/97.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

LOW TEMPERATURE METHOD FOR FORMING A THIN, UNIFORM OXIDE

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

David Denker, Reg. No. 40,987; Richard L. Donaldson, Reg. No. 25,673; William B. Kempler, Reg. No. 28,228; Jay M. Cantor, Reg. No. 19,906; Wade James Brady III, Reg. No. 32,080; Robby T. Holland, Reg. No. 33,304; and Christopher L. Maginniss, Reg. No. 30,288; and Carlton H. Hoel, Reg. No. 29,934

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
David Denker Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, Texas 75265	David Denker (972) 917-4388

NAME OF INVENTOR: (3)	NAME OF INVENTOR: (2)	NAME OF INVENTOR: (3)	NAME OF INVENTOR: (4)
Glen D. Wilk	Robert M. Wallace	Berinder P. S. Brar	
RESIDENCE & POST OFFICE ADDRESS: 9050 Markville Dr. #821 Dallas, TX 75243	RESIDENCE & POST OFFICE ADDRESS: 428 Park Bend Drive Richardson, TX 75081	RESIDENCE & POST OFFICE ADDRESS: 3924 Montrose Dr. Plano, TX 75025	RESIDENCE & POST OFFICE ADDRESS:
COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP: India	COUNTRY OF CITIZENSHIP:
SIGNATURE OF INVENTOR: Glen Wilk	SIGNATURE OF INVENTOR: Robert M Wallace	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: 10/13/98	DATE: 10/13/98	DATE:	DATE:

ATTORNEY'S DOCKET NO.

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David Denker Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, Texas 75265			David Denker (972) 917-4388
NAME OF INVENTOR: (3) Glen D. Wilk	NAME OF INVENTOR: (2) Robert M. Wallace	NAME OF INVENTOR: (3) Berinder P. S. Brar	NAME OF INVENTOR: (4)
RESIDENCE & POST OFFICE ADDRESS: 9050 Markville Dr. #821 Dallas, TX 75243	RESIDENCE & POST OFFICE ADDRESS: 428 Park Bend Drive Richardson, TX 75081	RESIDENCE & POST OFFICE ADDRESS: 3924 Montrose Dr. Plano, TX 75025	RESIDENCE & POST OFFICE ADDRESS:
COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP: India	COUNTRY OF CITIZENSHIP:
SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR: Berinder P.S. Brar	SIGNATURE OF INVENTOR:
DATE:	DATE:	DATE: 10/14/98	DATE: